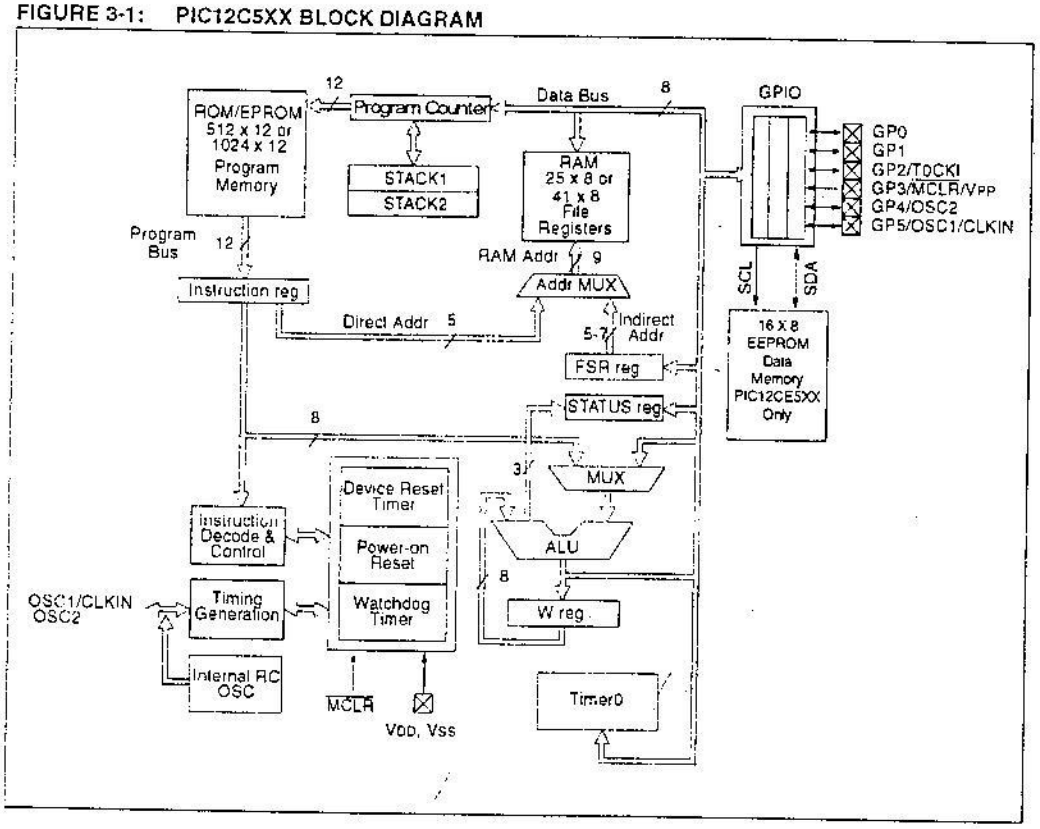
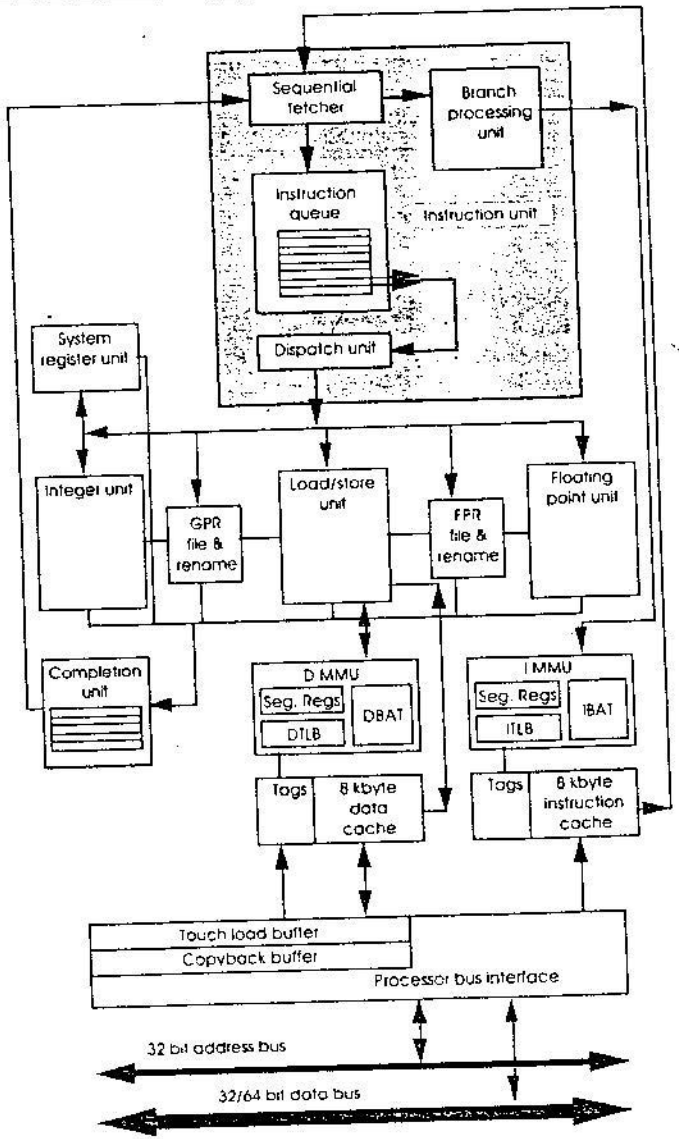
FIGURE 3-1: PIC12C5XX BLOCK DIAGRAM



The MPC603 block diagram

The MPC603 was the second PowerPC processor to appear. Like the MPC601, it has the three execution units: a branch unit to resolve branch instructions, an integer unit and a floating point unit.



MPC603 internal block diagram

The floating point unit supports IEEE format. However, two additional execution units have been added to provide dedicated support for system registers and to move data between the register files and the two onchip caches. The processor is superscalar and can dispatch up to three instruction and process five every clock cycle.

The branch unit supports both branch folding and speculative execution. It augments this with register renaming, which allows speculative execution to continue further than allowed on the MPC601 and thus increase the processing advantages of the processor.

The general purpose register file consists of 32 separate registers, each 32 bits wide. The floating point register file contains 32 registers, each 64 bits wide to support double precision floating point. The external physical memory map is a 32 bit address linear organisation and is 4 Gbytes in size.

The MPC603's memory subsystem consists of a separate memory management unit and on chip cache for data and instructions which communicates to external memory via a 32 bit address bus and a 64 or 32 bit data bus. This bus can, at its peak, fetch two instruction per clock or 64 bits of data. Each cache is 8 Kbytes in size, giving a combined on chip cache size of 16 Kbytes. The bus also supports split transactions, where the address bus can be used independently and simultaneously with the data bus to improve its utilisation. Bus snooping is also provided to ensure cache coherency with external memory.

As with the MPC601, the MPC603 speeds up the address translation process, by keeping translation information in one of four translation lookaside buffers, each of which is divided into two pairs, one for data accesses and the other for instruction fetches. It is different from the MPC601 in that translation tablewalks are performed in software and not automatically by the processor.

The device also includes power management facilities and is eminently suitable for low power applications.

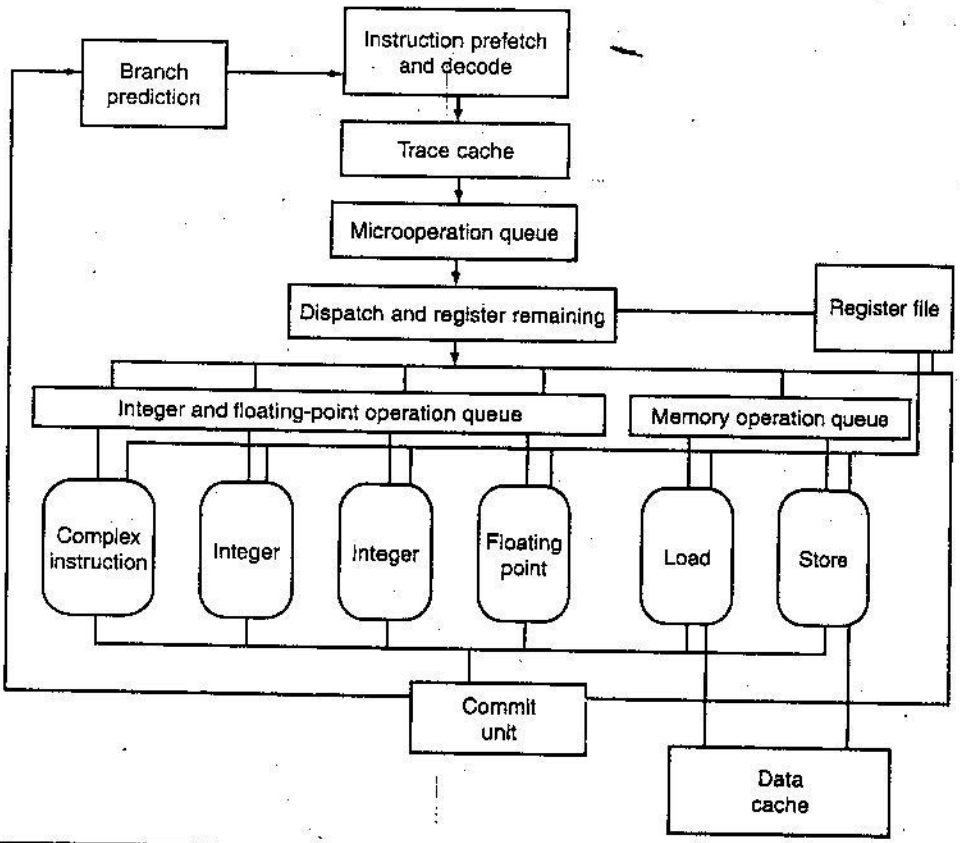


FIGURE 6.50 The microarchitecture of the Intel Pentium 4. The extensive queues allow up to 126 microoperations to be outstanding at any point in time, including 48 loads and 24 stores. There are actually seven functional units, since the FP unit includes a separate dedicated unit for floating-point moves. The load and store units are actually separated into two parts, with the first part handling address calculation and the second part responsible for the actual memory reference. The integer ALUs operate at twice the clock frequency, allowing two integer ALU operations to be completed by each of the two integer units in a single clock cycle. As we described in Chapter 5, the Pentium 4 uses a special cache, called the trace cache, to hold predecoded sequences of microoperations, corresponding to IA-32 instructions. The operation of a trace cache is explained in more detail in Chapter 7. The FP unit also handles the MMX multimedia and SSE2 instructions. There is an extensive bypass network among the functional units; since the pipeline is dynamic rather than static, bypassing is done by tagging results and tracking source operands, so as to allow a match when a result is produced for an instruction in one of the queues that needs the result. Intel is expected to release new versions of the Pentium 4 in 2004, which will probably have changes in the microarchitecture.

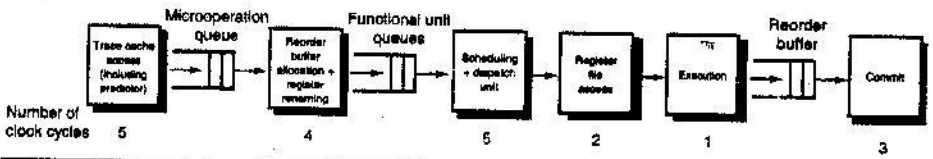


FIGURE 6.51 The Pentium 4 pipeline showing the pipeline flow for a typical instruction and the number of clock cycles for the major steps in the pipeline. The major buffers where instructions wait are also shown.